

TITLE OF THE INVENTION:

[0001] Circuit and Method for Controlling Gain in an Amplifier

BACKGROUND OF THE INVENTION:**Field of the Invention:**

[0002] Certain embodiments of the present invention relate generally to circuits configured to control amplifiers. Certain other embodiments of the present invention relate generally to methods for controlling amplifiers.

Description of the Related Art:

[0003] Wide-Band Received Signal Strength Indicator (WRSSI) circuits are commonly used in electronic systems that include mixers and amplifiers such as, for example, automatic-gain controlled amplifiers (ACG). In such systems, the WRSSI circuits control the gain of one or more of the amplifiers that are outside of the WRSSI circuit.

[0004] Commonly-used WRSSI circuits generally receive signals from an outside amplifier after the signals have passed through at least two mixers. For example, amplifier signals may be received by a WRSSI circuit from an I mixer and a Q mixer, whose outputs are 90° out-of-phase with each other. Common WRSSI circuits then process these signals independently through separate paths. Hence, since providing multiple paths requires the inclusion of redundant components, commonly-used WRSSI circuits are relatively large, require a considerable amount of power for operation, and are relatively difficult to cool. Further, currently-available WRSSI circuits are typically highly sensitive to variations in temperature, process, and power supply voltage.

SUMMARY OF THE INVENTION:

[0005] Certain embodiments of the present invention include electronic circuits for controlling the gain of a first amplifier that is operably connected to a circuit. According to certain embodiments of the present invention, such a circuit often include a first portion for receiving a first input signal and a second input signal from a second amplifier. Typically, this first portion produces a first output signal that is an inverse logarithmic function of a combination of the first input signal and the second input signal. Commonly, such circuits also include a second portion for digitally processing the first output signal and to produce a second output signal that controls the gain of the first amplifier.

[0006] Embodiments of the present invention also include methods of controlling gain in a first amplifier. Such methods include a step of receiving a first input signal and a second input signal from a second amplifier in a first portion of a circuit. Typically, such methods include a step of producing a first output signal in the first portion, wherein the first output signal is an inverse logarithmic function of a combination of the first input signal and the second input signal. Often, these methods also include the step of forwarding the first output signal to a second portion of the circuit and digitally processing the first output signal in the second portion to produce a second output signal. Normally, such methods also include the step of controlling the gain of the first amplifier using the second output signal.

[0007] According to yet other embodiments of the present invention, other circuits configured to control the gain of a first amplifier are provided. The circuits typically include receiving means or receiving a first input signal and a second input signal from a second amplifier. Generally, first production means are also included in such circuits for producing a first output signal

that is an inverse logarithmic function of a combination of the first input signal and the second input signal. In addition, such circuits often include processing means for digitally processing the first output signal and second production means for producing a second output signal that controls the gain of the first amplifier.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0008] For proper understanding of the invention, reference should be made to the accompanying drawings, wherein:

[0009] Figure 1 illustrates a schematic representation of a low-noise amplifier (LNA), a set of mixers, and a circuit configured to control the gain of the LNA;

[0010] Figure 2A includes a graph that illustrates the linear operation region of a circuit configured to control the gain of an outside amplifier, such as the LNA in Figure 1;

[0010] Figure 2B includes a graph that illustrates thresholds at which a circuit configured to control the gain of an outside amplifier switches the gain from high to low and from low to high;

[0011] Figure 3 illustrates a set of comparator circuits that may be included in a circuit configured to control the gain of an outside amplifier;

[0012] Figure 4 illustrates four-bit programmable resistive-divider-based circuitry that may be included in a circuit configured to control the gain of an outside amplifier; and

[0013] Figure 5 illustrates a flow chart that includes steps of a representative method for controlling the gain of an outside amplifier.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S):

[0014] Figure 1 illustrates first portion 100 and second portion 105 of a representative circuit according to an embodiment of the present invention. The representative circuit illustrated in Figure 1 is configured to control the gain of an amplifier outside of the circuit. For example, using the circuit illustrated in Figure 1, the gain of low-noise amplifier (LNA) 110 may be controlled.

[0015] Operably connected between LNA 110 and first portion 100 are two mixers 115 that are typically double-balanced I/Q mixers. Usually, mixers 115 are used to translate the frequency of signals forwarded by LNA 110 to the circuit before these signals reach first input 120 and second input 125 of first portion 100. In Figure 1, mixers 115 may take the form of a set of I & Q mixers that process differential signals from LNA 110. Typically, mixers 115 are driven by IQ linear oscillator (LO) signals that are 90° out-of-phase with each other, respectively.

[0016] First portion 100 is commonly referred to herein as the analog portion of the circuit illustrated in Figure 1 and typically includes several internal amplifiers and rectifiers. In the embodiment of the analog portion illustrated in Figure 1, three amplifiers 130, 135, 140 and five rectifiers 145, 150, 155, 160, 165 are operably connected to each other, to input ports 120, 125, and to output port 175 in the circuit. Signals from the rectifiers converge at Node A, where the signals are combined.

[0017] Also included in representative first portion 100 is capacitor 170. Capacitor 170, in combination with resistors 195, provides a resistor-capacitor (RC) filter that helps filter and smooth signals that are output from first portion 100 and forwarded to second portion 105.

[0018] While the circuit illustrated in Figure 1 is in operation, LNA 110 typically forwards Radio Frequency (RF) signals to mixers 115, and mixers

115 typically translate the RF signals into Intermediate Frequency (IF) signals that are forwarded to first portion 100. After receiving signals from mixers 115 at ports 120, 125, first portion 100 generally produces a first output signal that is emitted from portion 100 through output 175. Due to the rectifier configuration used in the circuit, this emitted signal is an inverse logarithmic function of a combination of the signals received at ports 120, 125.

[0019] In the device illustrated in Figure 1, when signals are received by both first input port 120 and second input port 125, because each port 120, 125 is electrically connected to amplifier 130 and rectifiers 145 and 150, a portion of each received signal travels into first amplifier 130, and a portion of each received signal travels into each of first rectifier 145 and second rectifier 150. Then, as mentioned above, at Node A, the above-listed portions of the signals are recombined into a single output signal that is then emitted from first output port 175 to input port 180 of second portion 105.

[0020] Second portion 105, which is referred to herein as a digital portion, is typically configured to receive, through input port 180, the single-ended output signal that is emitted from first output port 175. Second portion 105 is also typically configured to digitally process the output signal received from first portion 100 and to produce a second output signal that may be used to control the gain of LNA 110 and/or other outside amplifiers that may be operably connected, either directly or indirectly, to second portion 105. This second output signal is typically emitted from second portion 105 through second output port 185.

[0021] Also illustrated in second portion 105 in Figure 1 are resistors 195. These provide a connection between or, in other words, short, third input port 180 and voltage drain (VDD) which may, according to certain embodiments, equal the voltage of the power supply for the WRSSI circuit.

[0022] Second portion 105 usually includes at least one comparator circuit 187 and is generally configured to compare a value related to the first output signal received from first portion 100 (for example, a value related to the amplitude of the first output signal) to one or more threshold values. Commonly, when a threshold value is reached, the comparator circuit 187 is configured to at least initiate switching of the gain of an outside amplifier, such as LNA 110, either from high to low or from low to high, depending on what kind of threshold value has been reached.

[0023] In other words, as illustrated in Figure 2B, when an input signal at input port 120 and/or input port 125 reaches or exceeds a first input threshold value 200 (for example, 30mV in Figure 2B), the gain of the outside amplifier is switched between a high level and a low level. To effectuate this change, output port 175 forwards a signal that, after having passed through the amplifiers and rectifiers of analog portion 100, has a value that is at or below a first output threshold value (for example, 782mV). Then, portion 105 recognizes that a threshold has been reached and the gain of LNA 110 is switched from a high value to a low value.

[0024] Conversely, when the value of the input signal at input port 120 and/or input port 125 is equal to or lower than a second input threshold value 210 (for example, 3mV in figure 2B), output port 175 forwards a signal having a value at or above a second output threshold value (for example, 928 mV). Then, portion 105 again recognizes that a threshold has been reached, and the gain of LNA 110 is switched from low to high.

[0025] Figure 2A illustrates how a circuit such as, for example, the circuit illustrated in Figure 1, may convert the values of the signals received through first input port 120 and second input port 125 into an inverse logarithmic function of these received signals, after these signals have been processed by the amplifiers and rectifiers of analog portion 100 and have

been combined at Node A. It should be noted that the x-axis in Figure 2A uses a logarithmic scale while the y-axis in Figure 2A uses a linear scale.

[0026] In Figure 2A, the above-discussed first threshold value 200 and second threshold value 210 have been indicated on the x-axis and have vertical dotted lines B and C running therethrough, respectively. To the left of line B and to the right of line C, vertical dotted lines A and D are illustrated. The curve illustrated in Figure 2A descends linearly from top left to bottom right between lines A and D. However, to the left of line A and to the right of line D, the curve flattens out significantly. The region of the curve illustrated in Figure 2A between lines A and D is referred to herein as the “linear signal region”, wherein a relatively small change of the input signal amplitude causes a relatively large change of output signal that is linearly related thereto.

[0027] Outside of lines A and D, the circuit illustrated in Figure 1 is substantially less responsive to fluctuations in the input signal received, for example, from LNA 110. Hence, in order to avoid the regions outside of lines A and D, the circuit illustrated is preferably operated between lines B and C.

[0028] Figure 3 illustrates an example of a comparator circuit 187 which may be used according to certain embodiments of the present invention. As illustrated in Figure 3, two separate comparators 300, 310 are included in comparator circuit 187, and each of these comparators 300, 310 may be used with one of the above-discussed output threshold values. According to other embodiments of the present invention, a single comparator may be used, or more than two comparators may be used.

[0029] Comparator circuit 187 illustrated in Figure 3 includes two decision circuits 315, 320 that are operably connected to the comparators 300, 310. In comparator circuit 187, if either decision circuit 315, 320 specifies that

the gain of an outside amplifier operably (for example, LNA 110) connected to comparator circuit 187 should be switched, then the gain of the outside amplifier is switched accordingly. Otherwise, the outside amplifier is allowed to operate at the gain at which it was previously set.

[0030] Figure 4 illustrates a representative threshold circuit 400 according to an embodiment of the present invention that may be included in comparator circuit 187. As shown in Figure 4, threshold circuit 400 may be based on a resistive-divider circuit configured to specify a value of a threshold. In Figure 4, half of threshold circuit 400 stores data related to the value of a first threshold and the other half of threshold circuit 400 stores data related to the value of a second threshold. It will be appreciated by those skilled in the art that, in this example, data related to the values of additional thresholds may also be stored in threshold circuit 400 or in other similar circuits.

[0031] Threshold circuit 400 may be programmed in a manner that is independent of first portion 100 and/or second portion 105. For example, as illustrated in Figure 1, three-wire controller 190 may be used to program the threshold circuit 400 in comparator circuit 187. Also, each threshold value stored in threshold circuit 400 may be stored as multiple-bits. For example, 4-bit programming may be used to store each of the threshold values.

[0032] In the device illustrated in Figure 1, the value of the output signal from analog portion 100, which equals the value of the signal at input port 180 of digital portion 105, is compared with output threshold values provided by threshold circuit 400 in digital portion 105. For example, the value of the signal at input port 180 may be compared to the above-discussed 782 mV and 928 mV threshold values. Based on this comparison, a determination is made concerning whether or not the gain of the outside

amplifier that is operably connected to output port 185 of digital portion 105 should be modified.

[0033] Threshold circuit 400 may include resistors 410 and 420, which can provide a connection between (in other words, short) the threshold ports VTH_HL and VTH_LH of the set of comparator circuits shown in Figure 3 and VDD. Also, the comparator circuit shown in Figure 3 may compare the signal received at input port 180 (or “IN” in Figure 3) with threshold ports VTH_HL and VTH_LH. Hence, since all three of the ports discussed above are indirectly shorted to VDD through one or more resistors, all of the signals will experience substantially less variation as the voltage of a power supply operably connected to the circuit illustrated in Figure 1 and Figure 3 fluctuates over time. Therefore, the circuit illustrated in Figure 1 will control the gain of an outside amplifier, such as LNA 110, using a relatively steady output signal, even as the voltage of the power supply operably connected to the WRSSI circuit varies over time.

[0034] In order to stabilize the circuit illustrated in Figure 1 over temperature, the biasing circuits, illustrated in first portion 100 as combinations of amplifiers and rectifiers, are cascaded. Therefore, the configuration of the WRSSI circuit illustrated in Figure 1 provides for a high degree of stability of the signal output from second portion 105, even as the temperature and process related to the circuit illustrated in Figure 1 fluctuate over time. Usually, threshold values 200 and 210 illustrated in the example of Figure 2B do not change by more than $\pm 3\text{dB}$ over any of the temperature, power supply, or process ranges over which the circuit illustrated in Figure 1 may be operated.

[0035] Figure 5 illustrates a flow chart 500 that includes steps of a representative method for controlling gain of an outside amplifier using a circuit such as, for example, the circuit illustrated in Figure 1. Step 505

specifies mixing a first input signal and a second input signal after the first input signal and the second input signal have been generated by an amplifier.

In Figure 1, the first and second input signals of step 505 may be generated by LNA 110, which is outside of the circuit, and mixed by mixers 115.

[0036] Step 510 specifies receiving the first input signal and the second input signal, that are generally differential and 90° out-of-phase with each other, in a first portion of a circuit. In Figure 1, such input signals are received at ports 120 and 125 of analog portion 100.

[0037] Step 515 specifies producing a first output signal in the first portion. According to step 515, the first output signal is an inverse logarithmic function of a combination of the first input signal and the second input signal.

[0038] Step 520 in Figure 5 specifies forwarding the first output signal to a second portion of the circuit. In Figure 1, this second portion is represented as digital portion 105. According to step 525, digital processing of the first output signal in the second portion is performed to produce the second output signal. This digitally processing step includes comparing the first output signal to at least two switching thresholds, such as threshold values 200 and 210 illustrated in Figure 2A and discussed above.

[0039] According to step 530, controlling the gain of the amplifier may be performed using the second output signal. Step 535 specifies setting the at least two switching thresholds using resistive divider-based circuits. It should be noted that, according to step 540, 4-bit independent programmability may be provided for each switching thresholds illustrated here. It should be also noted that, according to step 545, fluctuation due to power supply variation of the second output signal may be reduced by shorting the second output signal to VDD. According to step 550, further

stability may be provided by providing cascaded mirror devices in the bias-reference circuit to reduce current fluctuation of the second output signal.

[0040] One having ordinary skill in the art will readily understand that the invention as discussed above may be practiced with steps in a different order, and/or with hardware elements in configurations which are different than those which are disclosed. Therefore, although the invention has been described based upon these preferred embodiments, it would be apparent to those of skill in the art that certain modifications, variations, and alternative constructions would be apparent, while remaining within the spirit and scope of the invention. In order to determine the metes and bounds of the invention, therefore, reference should be made to the appended claims.